WHAT IS CLAIMED IS:

1. A method of performing data string operations comprising:

routing a series of instructions to a general purpose microprocessor having a first execution unit for executing instructions;

analyzing said series of instructions so as to detect an instruction to perform a data string operation;

routing said instruction to perform a data string operation to a second execution unit separate from said first execution unit, wherein said second execution unit receives an undecoded version of said instruction;

controlling read and write operations to and from external memory with said general purpose microprocessor via control circuitry, wherein said external memory is external to said general purpose microprocessor; and

controlling read and write operations to and from external memory with said second execution unit via said control circuitry and without intervention by said first execution unit.

2. The method of Claim 1, wherein said first execution unit is on a first integrated circuit and wherein said second execution unit is on a second integrated circuit.

3. The method of Claim 2, wherein said second integrated circuit includes a bus interface unit in association with said second execution unit.

4. The method of Claim 2, wherein said second integrated circuit comprises a memory controller.

5. The method of Claim 4, wherein said act of routing said data string instruction to said memory controller comprises writing said data string instruction to an I/O address.

6. The method of Claim 5, wherein said I/O address is normally not used for I/O devices.

7. The method of Claim 1, additionally comprising checking the content of a data cache to determine if at least a portion of a data string which is the subject of said data string instruction is present in said data cache.

8. The method of Claim 7, wherein modified cache lines present in said data cache which contain data forming at least a portion of said data string are written back to main memory before or during the execution of said data string instruction.

9. A digital processing system optimized for string manipulations comprising:

an instruction fetch unit coupled to an external memory;

a first execution unit coupled to receive, decode, and perform assembly language arithmetic and logic instructions received from memory via said instruction fetch unit;

a second execution unit coupled to receive, decode, and perform assembly language string manipulation instructions received from memory via said instruction fetch unit; and

memory circuitry, external to said first and second execution units, configured to be alternatively controlled by said first execution unit and said second execution unit using the same memory control circuitry, wherein said first execution unit and said second execution unit are separately coupled to said memory control circuitry.

10. The digital processing system of Claim 9 additionally comprising a data cache, wherein said data cache stores a subset of that data which is stored in said memory, and wherein said second execution unit is coupled to said data cache and configured to maintain data cache coherency with said memory.

11. The digital processing system of Claim 10, additionally comprising a plurality of comparators having a first input coupled to said data cache and a second input coupled to a source of compare data.

12. The digital processing system of Claim 11, wherein said source of compare data comprises said second execution unit.

13. A processing system comprising:

a main memory for storing data and instructions;

a cache memory for storing a subset of said data stored in said main memory;

a first execution unit on a first integrated circuit, configured to perform arithmetic and logical instructions on data received from said main memory and said cache memory;

a memory controller on a second integrated circuit, coupled to said main memory and said first execution unit, comprising string execution circuitry configured to receive, decode, and perform assembly language string manipulation instructions on data from said main memory and said cache memory, wherein said memory controller is configured to control read and write operations to and from said main memory for both said string execution circuitry and said first execution unit; and

means for maintaining cache memory coherency with said main memory.

14. A processing system comprising:

an instruction fetch unit coupled to an external memory;

a first execution unit coupled to receive, decode, and perform assembly language arithmetic and logic instructions received from memory via said instruction fetch unit;

a second execution unit coupled to receive, decode, and perform assembly language string manipulation instructions received from memory via said instruction fetch unit;

memory circuitry, external to said first and second execution units; and

a bus interface unit, coupled to said memory circuitry, said first execution unit, and said second execution unit, wherein said memory circuitry is configured to be alternatively controlled by said first execution unit and said second execution unit via said bus interface unit, and wherein said second execution unit is configured to operate said memory circuitry independently of said first execution unit.

15. A method of performing data string operations comprising:

routing a series of individual assembly language opcodes to a general purpose microprocessor having a first execution unit for executing instructions;

analyzing said series assembly language opcodes so as to detect an instruction to perform a data string operation;

routing said instruction to perform a data string operation to a second execution unit separate from said first execution unit, wherein said instruction comprises at least one individual opcode for performing a data string operation, and wherein said second execution unit receives an undecoded version of said instruction;

controlling read and write operations to and from memory external to said general purpose microprocessor with said general purpose microprocessor via control circuitry; and

controlling read and write operations to and from said memory with said second execution unit via said control circuitry.

16. The method of Claim 15, wherein said first execution unit is on a first integrated circuit and wherein said second execution unit is on a second integrated circuit.

17. The method of Claim 16, wherein said second integrated circuit comprises a memory controller.

18. The method of Claim 17, wherein routing said instruction to perform a data string operation to said second execution unit comprises writing said data string instruction to an I/O address.

19. The method of Claim 18, wherein said I/O address is normally not used for I/O devices.

20. The method of Claim 15, additionally comprising checking the content of a data cache to determine if at least a portion of a data string which is the subject of said data string instruction is present in said data cache.

21. The method of Claim 20, wherein modified cache lines present in said data cache which contain data forming at least a portion of said data string are written back to main memory before or during the execution of said data string instruction.

22. A processing system comprising:

a host processing integrated circuit;

a separate memory integrated circuit;

a separate memory controller integrated circuit coupled between said host processing integrated circuit and said memory integrated circuit; and

dedicated string execution circuitry integral to said memory controller integrated circuit and configured to perform string manipulation instructions on data in said memory integrated circuit without intervention by said host processing integrated circuit.

23. The processing system of Claim 22, wherein said host processing integrated circuit comprises both a general purpose execution unit and a dedicated string execution unit.

24. A method of performing data string operations comprising:

routing a series of instructions to a general purpose microprocessor having a first execution unit for executing instructions;

analyzing said series of instructions with said first execution unit so as to detect an instruction to perform a data string operation; and

routing with the first execution unit said instruction to perform a data string operation to a second execution unit separate from said first execution unit, wherein said second execution unit receives an undecoded version of said instruction.

25. The method of Claim 24, wherein said first execution unit is on a first integrated circuit and wherein said second execution unit is on a second integrated circuit.

26. The method of Claim 25, wherein said second integrated circuit includes a bus interface unit in association with said second execution unit.

27. The method of Claim 25, wherein said second integrated circuit comprises a memory controller.

28. The method of Claim 27, wherein said act of routing said data string instruction to said memory controller comprises writing said data string instruction to an I/O address.

29. The method of Claim 28, wherein said I/O address is normally not used for I/O devices.

30. The method of Claim 26, additionally comprising checking the content of a data cache to determine if at least a portion of a data string which is the subject of said data string instruction is present in said data cache.

31. The method of Claim 30, wherein modified cache lines present in said data cache which contain data forming at least a portion of said data string are written back to main memory before or during the execution of said data string instruction.

32. A method of performing data string operations comprising:

routing a series of instructions to a general purpose microprocessor having a first execution unit;

analyzing said series of instructions so as to detect an instruction to perform a data string operation; and

routing said instruction to perform a data string operation to a second execution unit such that said first execution unit does not receive said instruction.

33. The method of Claim 32, wherein said first execution unit is on a first integrated circuit and wherein said second execution unit is on a second integrated circuit.

34. The method of Claim 33, wherein said second integrated circuit includes a bus interface unit in association with said second execution unit.

35. The method of Claim 33, wherein said second integrated circuit comprises a memory controller.

36. The method of Claim 35, wherein said act of routing said data string instruction to said memory controller comprises writing said data string instruction to an I/O address.

37. The method of Claim 36, wherein said I/O address is normally not used for I/O devices.

38. The method of Claim 32, additionally comprising checking the content of a data cache to determine if at least a portion of a data string which is the subject of said data string instruction is present in said data cache.

39. The method of Claim 38, wherein modified cache lines present in said data cache which contain data forming at least a portion of said data string are written back to main memory before or during the execution of said data string instruction.

40. The method of Claim 32, wherein analyzing said series of instructions is performed by an instruction fetch unit.